Roll No. .....

Subject Code—6757-X

P.G.D.C.A./M.C.A. EXAMINATION

(MCA 3 Years)

(Second Semester)

(Re-appear Batch Prior to 2009)

MS-07

COMPUTER ORG. & ARCH.

Time : 3 *Hours* *Maximum Marks* : 100

Note : Attempt any *Five* questions. All questions carry equal marks.

1. (a) Explain software and hardware interaction layers in computer architecture.

   (b) Classify computer on the basis of instruction set. Also explain working principle of RISC and CISC type computers.

2. (a) Explain various addressing modes used in 8086 microprocessor.

(b) Differentiate microprogramming and hardwired control giving suitable examples.

3. (a) A two way set associative cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 128 K×32 :

(i) Formulate all pertinent information required to construct the cache memory.

(ii) What is the size of the cache memory ?

(b) Explain programmed, interrupt and DMA methods of data transfer techniques.

4. (a) Explain different memory organization techniques. Also discuss associative and virtual memory.

(b) Describe microprogram sequencer for a control memory.

5. (a) Explain four possible hardware schemes that can be used in an instruction pipeline in order to minimize the performance degradation caused by instruction branching.

(b) Show a block diagram for the data transfer from a CPU to an interface and then to an I/O device. Determine a procedure for setting and clearing the flag bit.

6. (a) Explain architectural aids to implement virtual memories.

(b) Explain the process of address selection for control memory.

7. (a) How many types of interrupts are there ? Differentiate among them.

(b) Discuss memory array organization. Also explain memory hierarchy.

8. Write short notes on the following :

(i) Transaction Processing benchmarks

(ii) Pipelining in CPU design

(iii) Superscalar processors

(iv) Design of control unit.