Roll No. .....

Subject Code—6801

M.C.A. (Second Year) EXAMINATION

(5 Years Integrated Course)

(Main Batch 2009)

MCA-204

COMPUTER ORGANIZATION AND ARCHITECTURE

Time : 3 *Hours* *Maximum Marks :* 70

Note : Attempt any *Five* questions. All questions carry equal marks.

1. (a) Design a four bit binary subtractor.
   (b) Design a four bit binary decrementer.

2. Explain the shift micro operations with suitable examples.

3. Explain the instruction cycle required for the execution of the instruction.

4. (a) Give the architecture of general register organization for 16 registers used for the design.

(b) Give the role of status bit for program control.

5. (a) Differentiate between RISC and CISC.

(b) Discuss the importance of priority interrupt for the I/O device handling.

6. (a) Draw a space-time diagram for a six-segment pipeline showing the time it takes to process eight tasks.

(b) A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six segment pipeline with a clock cycle of 10 ns. Determine the speed up ratio of the pipeline for 100 tasks. What is the maximum speed up that can be achieved ?

7. (a) The access time of cache memory is 100 ns and that of main memory 1000 ns. It is estimated that 80 per cent of the memory requests are for read and remaining 20 per cent for write. The hit ratio for read accesses only is 0·9. A write-through procedure is used :

(i) What is the average access time of the system considering only memory read cycles ?

(ii) What is the average access time of the system for both read and write requests ?

(iii) What is the hit ratio taking into consideration the write cycle ?

(b) An address space is specified by 24 bits and the corresponding memory space by 16 bits :

(i) How many words are there in the addressing space ?

(ii) How many words are there in memory space ?

(iii) If a page consists of 2 K words, how many pages and blocks are there in the system ?

8. Write short notes on the following :

(a) DMA controller

(b) Vector Processor.