June – 2008

Roll No. .....

Subject Code—9488

M.C.A. (Fifth Year) EXAMINATION

(5 Years Integrated Course)

MCA-502

ADVANCED ARCHITECTURE AND PARALLEL PROCESSING

Time : 3 Hours *Maximum Marks : 100*

Note : Attempt any *Five* questions. All questions carry equal marks.

1. (a) Characterize the architectural operation of multivector and SIMD computers. **10**

   (b) Distinguish between multiprocessors and multicomputers based on their structures resources sharing and interprocess communications. Also explain the differences among UMA, NUMA and COMA and NORMA computers. **10**

2. (a) Prove that the best parallel algorithm written for an n-processor EREW-PRAM model can be no more than O(log n) times slower than any algorithm for a CRCW model of PRAM having same number of processors. **10**

(b) Consider the multiplication of two n-bit binary integers using a 1·2 μm, CMOS multiplier chip. Prove the lower bound $AT^2 > Kn^2$, where A is chip area, T-execution time, n-word length and K is a technology dependent constant. **10**

3. (a) Define the following terms for various system interconnect architectures : **10**

(i) Node degree

(ii) Network diameter

(iii) Dynamic connection networks

(iv) Mesh *Vs.* Torus

(v) Multistage Networks.

(b) Perform a data dependency analysis on each of the following Fortran program fragments. Show the dependence graph among the statements with justification :

(i) S1 : A = B + D
S2 : C = A × 3
S3 : A = A + C
S4 : E = A/2

(ii) S1 : X = SIN(Y)
S2 : Z = X + W
S3 : Y = – 2·5 × W
S4 : X = cos (Z) **10**

4. Answer the following questions related to multistage networks : **20**

(a) How many legitimate states are there in a 4×4 switch module, including both broadcast and permutations ? Justify your answer with reasoning.

(b) Construct a 64-bit omega network using 4×4 switch module in multiple stage. How many permutations can be implemented directly in a single pass through the network without blocking.

(c) What is the percentage of one-pass permutations compared with total number of permutations achievable in one or more passes through the network.

5. Explain the structures and operational requirements of the instruction pipelines used in CISC, scalar RISC, superscalar, RISC and VLIW processors. Comment on the cycles per instruction expected from these processor architectures. **20**

6. Explain the following terms associated with cache and memory architectures : **5×4**

   (a) Low-order memory interleaving

   (b) Physical address cache *Vs.* Virtual address cache

   (c) Atomic *Vs.* Non-atomic memory accesses

   (d) Memory bandwidth and fault tolerance.

7. Consider the execution of a program of 15.000 instructions by a linear pipeline processor with a clock rate of 25 MHz. Assume that the

instruction pipeline has five stages and one instruction is issued per clock cycle. The penalties due to branch instructions and out-of-sequence execution are ignored.

   (a) Calculate the speedup factor in using this pipeline to execute the program as compared with the use of an equivalent non-pipelined processor with an equal amount of flow through delay. **10**

   (b) What are the efficiency and throughput of this pipelined processor ? **10**

8. Explain the following terms associated with multicomputer networks and message passing mechanism :

   (a) Message, packets and flits

   (b) Virtual channels *Vs.* Physical channels

   (c) Buffering flow control using virtual cut through routing

   (d) Virtual networks and sub networks.

5×4