Roll No. .....

Subject Code—2066-X

# M.C.A. EXAMINATION

(Fifth Semester)

(Re-appear)

MS-33

## ADVANCED COMPUTER ARCHITECTURE

*Time* : 3 *Hours* *Maximum Marks* : 100

**Note** : Attempt any *Five* questions. All questions carry equal marks.

1. (a) Right from ENIAC system, the scientists have been developing systems to bring in parallelism. Discuss the evolution. 5

   (b) Differentiate between MIMD and SISD using block diagram. 5

   (c) Differentiate multiprocessors and multicomputers. 5

   (d) Differentiate scalar, superscalar and superpipelined architecture. 5

P.T.O.

2. (a) Explain with suitable example, detection of parallelism in a program using Bernstein's conditions. Also explain various dependencies such as resource and control dependencies. **10**

(b) What do you understand by PRAM model ? Briefly discribe various categories of PRAM models. Which category is the weakest and which is the strongest version and why ? **10**

3. (a) What are the significance of diameter and bisection width of a network ? Determine these parameters for a 3-D cube network. **10**

(b) Describe a 8×8 omega network using (2×2) switches. Show diagram depicting broadcasting capabilities of the network. **10**

4. (a) Explain the following terms associated with cache and memory architecture :

(i) Low-order memory interleaving

(ii) Physical address cache *versus* Virtual address cache. **5+5**

(b) Explain the following terms associated with cache design :

(i) Write through *versus* Write-back caches

(ii) Cache flushing policies. **5+5**

5. Consider the following reservation table for a five-stage pipeline with a clock period $\tau$.

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| $S_1$ | X | | | | | X |
| $S_2$ | | X | | | X | |
| $S_3$ | | | X | | | |
| $S_4$ | | | | X | | |
| $S_5$ | | X | | | | X |

(a) List the set of forbidden latencies and collision vector.

(b) Draw a state transition diagram showing all possible initial sequences without causing collision in the pipeline.

(c) List all the simple cycles from the state diagram.

(d) Identify the greedy cycles amongst the simple cycles and determine MAL.

(e) Evaluate the maximum throughput of the pipeline. 4+4+4+4+4

6. Depict and compare through figures the efficiency of the following architecture :

(a) Scalar and Superscalar

(b) Pipeline and Superpipelined

(c) Scalar and Vector Processor

(d) Scalar and VLIW processor. 5+5+5+5

7. (a) Describe inclusion, coherence and locality of reference properties of a memory hierarchy. 10

(b) What is virtual memory and why is it needed ? Discuss various address translation mechanism in a virtual memory environment. 10

8. Write notes on any *two* of the following :

(a) RISC *versus* CISC architecture

(b) Degradation of the efficiency of the pipeline as an effect of branch instruction and its solutions

(c) Data flow architecture

(d) Future is evolving towards high performance computing through MPP (Massively Parallel Processing). Discuss.

(e) Describe Grid Computing. **10,10**